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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/658,114	BILYALOV ET AL.	
	Examiner	Art Unit	
	Thanh-Truc Trinh	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 37-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 37-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1, 3-23, 26, 37-38, 40-42 and 45-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Stalmans et al. (US Patent 6683367).

Regarding claim 1, Stalmans et al disclose a photovoltaic device comprising a first layer, or non-porous layer 3 or 15, having a first semiconductor material of first conductivity type in one region (See col. 3 lines 1-9 or claim 1); a second layer, or substrate 1 or 13, having a second semiconductor material of a second conductivity type (See col. 4 lines 17-19, claim 20), wherein the second conductivity type is opposite the first conductivity type; a third layer (porous Si 2 or 14) having a third semiconductor material and situating between the first layer and the second layer. The third layer is

porous, translucent and acts as a diffusion barrier. (See Figures 1A-B, 7, 9, and col. 2 lines 32-47).

Regarding claim 3, Stalmans et al describe the photovoltaic device is a solar cell (See claim 22).

Regarding claims 4-7, Stalmans et al teach that the first, second and third semiconductor material comprise silicon. In other words, they all comprise a same semiconductor material and element. (See claims 2, 4 and 20)

Regarding claims 8-10, Stalmans et al teach that the second and third semiconductor materials comprise silicon. (See claims 20, 2).

Regarding claims 11-13, Stalmans et al teach that the first and third semiconductor materials comprise silicon. (See claims 4, 2).

Regarding claims 14-16, Stalmans et al teach that the first and the second semiconductor material comprise silicon. (See claims 4, 20).

Regarding claims 17-19, Stalmans et al describe that the porous layer is etched from silicon wafer. (See col. 7 lines 63-67). Therefore, the porous layer comprises silicon which is inherently non-doped. In addition, silicon wafer is generally crystalline, either monocrystalline or multicrystalline.

Regarding claims 20-21, Stalmans et al describe the second layer (or the substrate) can be a silicon wafer. (See col. 7 lines 63-67). In addition, silicon wafer is either monocrystalline or multicrystalline semiconductor material.

Regarding claim 22, Stalmans et al describe the first layer comprises a thickness of from about 0.1 μm to 10 μm (See claim 9). This first layer or non-porous layer further

divides into two sub-layers, therefore the thickness of the sub-layer with opposite conductivity to the second layer (or the substrate) is inherently in the range of less than 0.1 μm to less than 10 μm. A thickness of less than 0.1 mm is well within the claimed range of about 3nm to about 100nm. Note: 0.1 mm = 100 nm.

Regarding claim 23, Stalmans et al disclose a dielectric layer of silicon nitride in place of non-porous layer, or first layer, on porous silicon layer. (See col. 10 lines 46-49 and claim 16). In other words, the photovoltaic device as described in claim 1 further comprises an amorphous silicon layer situating between the first and the third layer.

Regarding claim 26, Stalmans et al teach that the substrate (or second layer) is etched to form porous layers within the substrate (See col. 8 lines 25-33). The porosity changes gradually from bottom to top. (See col. 3 lines 10-14 or col. 10 lines 63-67 and col. 11 lines 1-4 or claim 6, 12-13).

Regarding claims 37, Stalmans et al. disclose a photovoltaic device wherein the third layer comprises a porous semiconductor material (silicon) as described in claim 1. Stalmans et al. also describe the porosity of the third layer, or the percentage of a total volume occupied by voids, is from 20% to 70% (See col. 3 lines 25-26), which is well within the range of 10% to 85% of the instant claim.

Regarding claim 38, Stalmans et al describe that the porous layer is etched from silicon wafer. (See col. 7 lines 63-67 bridging col. 8 lines 1-46). Therefore, the porous layer comprises silicon which is inherently non-doped. In addition, silicon wafer is generally crystalline, either monocrystalline or multicrystalline.

Regarding claims 40-42 and 45-46, Stalmans et al. describe the porous silicon layer having light diffusing property (See col. 2 lines 50-52) and acting as a barrier to prevent diffusion of impurities (See col. 5 lines 51-58). Further, Stalmans et al. describe the porosity being formed by chemical etching (See col. 8 lines 1-46) and the degree of porosity can be tuned from 20% to 70% (See col. 3 lines 24-26). As seen in Figures 1(a) and 1(b), Stalmans et al. also depict an arrow representing light going through the porous silicon layer 2. Therefore, it is the Examiner's position that the third layer (or porous silicon layer) is translucent and acts as a diffusion barrier. It is also the Examiner's position that the porous silicon layer of Stalmans et al. can be highly transparent, because the degree of transparency depends on the porosity of the porous silicon layer.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 2, 24-25, 39 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stalmans et al in view of Fathauer et al (US Patent 5757024).

Regarding claims 2, 43-44, Stalmans et al disclose a photovoltaic device, wherein the porous layer is translucent and acts as a diffusion barrier as described in claim 1. Stalmans et al. also describe the first layer comprises a thickness of from about 0.1 μm to 10 μm (See claim 9). This first layer or non-porous layer further divides into two sub-layers, therefore the thickness of the sub-layer with opposite conductivity to the second layer (or the substrate) is inherently in the range of less than 0.1 μm to less than 10 μm. A thickness of less than 0.1 μm is well within the claimed range of about 3nm to about 100nm. Note: 0.1 μm = 100 nm.

Stalmans et al do not explicitly teach that the thickness of the porous semiconductor layer is from about 1nm to about 50 nm.

Fathauer et al teach that the thickness of porous silicon is in the range of 5 to 20 nm. This would eliminate detrimental porosification in the non-porous silicon layers. (See col. 3 lines 23-28).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Stalmans et al by having the thickness of porous layer of about 5 nm to about 20 nm as taught by Fathauer et al, because it would eliminate detrimental porosification (See col. 3 lines 24-26).

Regarding claims 24-25, Stalmans et al disclose a photovoltaic device as described in claim 1.

Stalmans et al do not teach about the fourth layer of porous semiconductor material attaching to the second layer (or the substrate). Stalmans et al also do not teach that there is a fifth layer of semiconductor material comprising the same conductivity type with the fourth layer and attaching to the fourth layer, wherein the fifth layer comprises a material selected from the group consisting of amorphous silicon, nanocrystalline, and microcrystalline semiconductor.

Fathauer et al teach multiple alternating layers of monocrystalline semiconductor with a thickness in nanometer (See col. 3 lines 50-54) and thin porous Si-Ge. These layers have silicon as their primary semiconductor material. Without doping material, they are inherently having the same conductivity type. (See abstract or col. 6 lines 56-67 and col. 7 lines 1-18 and Figures 1-2)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Stalmans et al by forming multiple alternating layers of silicon and porous silicon-containing, because it would increase the efficiency and the use of the device. (See col. 9 lines 37-49)

6. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stalmans et al. (US Patent 6683367) in view of Iwamoto et al. (US Patent 5066340).

Regarding claim 39, Stalmans et al. disclose a photovoltaic device as described in claim 1, wherein the first and second layers have opposite conductivities, and the third layer consists a porous non-doped silicon semiconductor material.

Stalmans et al. do not explicitly teach the second and third layers comprising a multicrystalline silicon semiconductor, nor do they teach the first layer comprises an amorphous silicon semiconductor.

Iwamoto et al. teach a photovoltaic device with an intrinsic multicrystalline layer 2 sandwiching between a p-type multicrystalline silicon layer 1 and an n-type amorphous silicon layer 3. (See Figure 1, col. 2 lines 60-68 bridging col. 3 lines 1-10 and col. 2 lines 44-59).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Stalmans by using multicrystalline silicon semiconductor for the second and porous layer, and amorphous silicon for the first layer as taught by Iwamoto et al., because it would provide a device with higher conversion efficiency and can be manufactured economically. (See col. 1 lines 57-60)

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 1, 3, 4-23, 38-42 and 45-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada et al. (US Patent 5331180).

Regarding claims 1, 40-42 and 45-46, Yamada et al disclose a photovoltaic device (See Figure 4) comprising a first layer of first semiconductor material of first conductivity type 42; second layer of second semiconductor material of a second conductivity type 12, wherein the second conductivity type is opposite to the first conductivity type; and a third layer 22 situating between the first and the second layers, wherein the third layer is porous, translucent (See col. 8 lines 36-47, 66-68) and behaves like a diffusion barrier. (See abstract). The porous layer is in form of wires vertically arranged and able to emit light (See Figure 1B and col. 3 lines 12-14), therefore it is the Examiner's position that the porous layer is translucent and highly transparency.

Regarding claim 3, Yamada et al describe the photovoltaic device is a photodiode (See col. 3 lines 12-14 or claim 1).

Regarding claims 4-7, Yamada et al teach that the first, second and third semiconductor material comprise silicon. In other words, they all comprise a same semiconductor material and element. (See col. 8 lines 36-47, 66-68)

Regarding claims 8-10, Yamada et al teach that the second and third semiconductor materials comprise silicon. (See col. 8 lines 36-47).

Regarding claims 11-13, Yamada et al teach that the first and third semiconductor materials comprise silicon. (See col. 8 lines 36-47, 66-68).

Regarding claims 14-16, Yamada et al teach that the first and the second semiconductor material comprise silicon. (See col. 8 lines 36-47, 66-68).

Regarding claims 17-19, Yamada et al describe that the porous layer is etched from polycrystalline silicon. (See col. 8 lines 43-47). Therefore, the porous layer comprises crystalline silicon, and the silicon itself is inherently non-doped.

Regarding claims 20-21, Yamada et al describe the second layer 12 is a polycrystalline Si layer. (See col. 8 lines 39-47).

Regarding claim 22, Yamada et al. describe the first layer 42 having thickness of 500 angstroms or 50 nm (See col. 8 lines 66-68), which is well within the claimed range of 3nm to 100 nm.

Regarding claim 23, Yamada et al. disclose an amorphous SiO_2 layer 32 on top of porous layer 22 and below the semiconductor layer 42, or between the first and third layers. (See Figure 4 and col. 8 lines 47-51)

Regarding claim 38, Yamada et al. describe the third layer (or the porous silicon 22) being formed from a polycrystalline Si 12, and subjected to an anodic oxidation.

(See col. 8 lines 39-47). Therefore, it is the Examiner's position that the porous silicon layer consists of a porous non-doped polycrystalline silicon semiconductor material. (See col. 3 lines 15-27).

Regarding claim 39, as seen in Figure 4 and col. 8 lines 36-68, Yamada et al. disclose the second layer (12) comprising the second layer of polycrystalline silicon semiconductor materials of p-type conductivity; the first layer (42) of polycrystalline (or multicrystalline) silicon semiconductor materials of n-type conductivity, wherein the "polycrystalline Si" includes "amorphous Si" (See col. 21 lines 34-38); the third layer 22 consists of a porous silicon semiconductor material comprising a multicrystalline semiconductor situated between the first layer and the second layer. Yamada et al. also describe the porous layer (or quantum wires) being intrinsic (i layer) (See col. 3 lines 15-27). In other words, the porous layer is also non-doped.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 2, 24-25 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al in view of Fathauer et al (US Patent 5757024).

Regarding claims 2 and 43-44, Yamada et al disclose a photovoltaic device as described in claim 1, wherein the first layer (42) has a thickness of 500 angstrom or 50nm. (See col. 8 lines 66-68).

Yamada et al do not explicitly teach that the thickness of the porous semiconductor layer is from about 1nm to about 50 nm.

Fathauer et al teach that the thickness of porous silicon is in the range of 5 to 20 nm. Limiting the thickness of porous layer would eliminate detrimental porosification in adjacent silicon layers (See col. 3 lines 23-28).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Yamada et al by having the thickness of porous layer of about 5 nm to about 20 nm as taught by Fathauer et al, because it would eliminate detrimental porosification. (See col. 3 lines 25-27)

Regarding claims 24-25, Yamada et al disclose a photovoltaic device as described in claim 1.

Yamada et al do not teach about the fourth layer of porous semiconductor material attaching to the second layer (or the substrate). Yamada et al also do not teach that there is a fifth layer of semiconductor material comprising the same conductivity type with the fourth layer and attaching to the fourth layer.

Fathauer et al teach multiple alternating layers of monocrystalline semiconductor with a thickness in nanometer (See col. 3 lines 50-54) and thin porous semiconductor. These layers have silicon as their primary semiconductor material. Without doping, these layers inherently have the same conductivity type. (See abstract or col. 6 lines 56-67 and col. 7 lines 1-18 and Figures 1-2)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Yamada et al by forming multiple alternating layers of silicon and porous silicon-containing, because it would increase the efficiency and the use of the device. (See col. 9 lines 37-49)

12. Claim 26 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al in view of Stalmans et al (US Patent 6683367).

Regarding claim 26, Yamada et al disclose a photovoltaic device as described in claim 1 with a porous semiconductor sandwiching between two semiconductor layers with different conductivity types.

Yamada et al do not teach forming plurality of macro etch pits with diameter changing from greater than 1 micron to less than 1 micron.

Stalmans et al teach that the substrate (or second layer) is etched to form porous layers within the substrate (See col. 8 lines 25-33). The porosity changes gradually from bottom to top. (See col. 3 lines 10-14 or col. 10 lines 63-67 and col. 11 lines 1-4 or claims 6, 12-13)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Yamada et al by etching pits with different sizes as taught by Stalmans et al, because beside allowing high-quality epitaxial semiconductor growing, it would also exhibit sufficient strong light diffusion and reflecting. (See col. 11 lines 1-4)

Regarding claim 37, Yamada et al. disclose a photovoltaic device as described in claim 1.

Yamada et al. do not explicitly teach the percentage of a total volume occupied by voids is from 10% to 85%.

Stalmans et al. teach the porosity of the porous silicon semiconductor layer is typically from 20% to 70%. (See col. 3 lines 25-26)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify to device of Yamada et al. by having the porous silicon layer with porosity from 20% to 70% as taught by Stalmans et al., because it would

provide a desired performance in term of overall efficiency of the device. (See col. 3 lines 26-28)

Response to Arguments

Applicant's arguments filed 03/27/2007 have been fully considered but they are not persuasive.

Applicant argues that Stalmans et al. do not disclose a third layer comprising a translucent layer. The Examiner respectfully disagrees. As seen in Figures 1(a) and 1(b), Stalmans et al. depict that the porous silicon layer can transmit light by showing an arrow (representing light) passing through the porous layer 2. Stalmans et al. also describe the porous silicon layer being formed by chemical etching (See col. 8 lines 1-46). Accordingly, channels are typically formed through the unmasked areas, thereby transmitting light. It is the Examiner's position that Stalmans et al. clearly teach the limitation of the porous silicon comprising a translucent layer. It is also the Examiner's position that the structural limitations and material of making are clearly taught by Stalmans et al., thus the claimed characteristics of the structural limitation are inherent.

Applicant argues that Fathauer et al. disclose an optically transparent top contact 68 and that this contact is not porous and is not situated between a first layer and second layer of opposite conductivities. However, this argument is deemed to be irrelevant. Fathauer et al. teach a buried porous semiconductor layer situated between two monocrystalline silicon layer and lattices of alternating layers of monocrystalline silicon and porous semiconductor. (See the Abstract of Fathauer et al.). Fathauer et al.

teach the thickness of this porous semiconductor is in the range of 5 to 20 nm (See col. 3 lines 23-28) which is used by the Examiner to combine with Stalmans in 103(a) rejection. Top contact 68 has nothing to do with the porous semiconductor layer having thickness from 5 to 20 nm. In addition, as seen in Figure 6 of Fathauer et al., the Examiner believe that the porous semiconductor layer 62 made of SiGe is intended to have a thickness between 5 to 20 nm, not the contact layer 68.

Applicant further argues that layer 22 of Yamada et al. is not a translucent layer but instead of a light emitting layer. Applicant also argues that Yamada disclose a transparent conductive films that are transparent but formed on the surface of the porous semiconductor layer and are not part of the porous semiconductor layer. As seen in Figure 1B, Yamada et al. show an enlarged porous semiconductor region, which has a form of vertical wires with opening channels between the wires. These opening channels of the porous silicon layer can inherently transmit light, or the porous silicon layer 22 is translucent. Further, the porous silicon layer 22 of Yamada et al. must be translucent since it is a light emitting layer. The transparent conductive films pointed out by the Applicant have nothing to do with the claimed limitations.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: US Patent 5272355.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh-Truc Trinh whose telephone number is 571-272-6594. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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06/02/07

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